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ULTRA-THIN SOI MOSFET METHOD AND STRUCTURE

Abstract

An ultra-thin, scaleable MOSFET transistor and fabrication method are described. The transistor features fully self-aligned, raised source/ drain junctions on a thin SOI wafer and exhibits low contact resistance, low gate resistance and good device isolation characteristic. No extra lithographic mask steps are required beyond those required by conventional processes. The transistor is completely "bracketed" or surrounded by STI (shallow trench isolation), providing inherent isolation between it and any other devices on the SOI wafer. Gate sidewall spacers are formed outside of the gate area so that the scalability is limited solely by lithography resolution.